IN THE CLAIMS:

1. (Currently Amended) An electronic memory component or memory module, ~~having~~comprising:

at least one memory cell area comprising memory blocks in which physical states ~~representing~~represent regular data; ~~are mapped by~~

mapping means for distinguishing unwritten memory blocks from previously written memory blocks by providing ~~of~~ at least one mapping function between physically implemented bits (P) and logically read bits (K) that describes at least one error correction code associated with one of the unwritten or previously written memory blocks, ~~for example at least one Hamming code,~~and

~~characterized by~~ at least one ~~further~~additional physical state of the memory cell in addition to the physical states that represent regular data,~~representing~~ said at least one additional physical state comprising attributes identified by the error correction code as at least one exceptional or special state ~~in the error correction code~~ (S,L) of data other than regular data.

2. (Currently Amended) ~~A~~ The memory component or memory module as claimed in claim 1, ~~characterized in that~~wherein the error correction code ~~and/or the possible reactions to the various physical states are~~ is implemented using hardware and/or software; and

wherein the at least one error correction code comprises at least one Hamming Code.

3. (Currently Amended)~~A~~ The memory component or memory module as claimed in claim 1, ~~characterized in that~~wherein the at least one additional physical state identified by the error correction code as an exceptional or special state ~~in the error correction code is given by the~~ comprises at least one of:

(i) a flow of leakage currents while memory cell transistors of any one bit are switched off;

(ii)~~as~~ a memory block or memory cell area which has not yet been written;

(iii)~~by manipulating~~a ~~the~~ memory cell area, ~~for example by irradiating the memory cell area~~ irradiated with electromagnetic particles or waves;

(iv) ~~and/or by the~~ erasure of ~~a~~a memory block or a memory cell area.

4. (Currently Amended) ~~A~~The memory component or memory module as claimed in at least one of claim 1, ~~characterized in that~~wherein the error correction code is configured as at least one Hamming code, which is designed for correcting one-bit errors in the memory cell area and has a Hamming distance of 3, so that each valid ~~code word or data~~ word differs from any other ~~code word or data~~ word in at least three bits, and in that for each eight-bit ~~code word or data~~ word ~~additionally~~ at least four redundant bits are provided, resulting in twelve-bit ~~code words or data~~ words.

5. (Currently Amended)~~A~~ The memory component or memory module as claimed in claim 4, ~~characterized in that~~wherein the Hamming code is designed such that each valid twelve-bit ~~code word or data~~ word has at least two ~~set~~ bits that are set at a predetermined level and/or at least two ~~erased~~ bits that have been erased, so that each

valid twelve-bit ~~code word or data~~ word has a minimum Hamming distance of 2 for special states in which all bits of a byte are set, or in which all bits of a byte are erased.

6. (Currently Amended) ~~A~~ The memory component or memory module as claimed in claim 4, ~~characterized in that~~

wherein the four redundant bits of the twelve bit word in the test mode, ~~which also~~ comprises states in which all bits of a byte are set or in which all bits of a byte are erased, are selected as follows:

(a) a third redundant bit R3 having a same ~~corresponds to~~ parity ~~of the~~as a seventh data bit, ~~of the~~a sixth data bit,- a ~~of the~~ fifth data bit, ~~of the~~a fourth data bit and ~~of the~~a first data bit;

(b) a second redundant bit R2 having a same ~~corresponds to~~ having a same parity ~~of the~~as the seventh data bit, ~~of the~~the sixth data bit, ~~of the~~a third data bit, ~~of the~~a second data ~~of the~~and a zero data bit;

(c) a first redundant bit ~~corresponds~~R1 having a same ~~to~~ parity ~~of the~~as the seventh data, ~~of~~ the fifth data bit, ~~of~~ the fourth data bit, ~~of~~ the third data bit, and ~~of~~ the zero data bit;

(d) a zero redundant bit R0 ~~corresponds to~~having a same parity ~~of~~ as the sixth data bit, ~~of~~ the fourth data bit, ~~of~~ the third data bit, ~~of~~ the second data bit ~~of~~and the first data bit; and/or

wherein in ~~the~~ a normal mode are the twelve bit words are selected as follows:

(e) a third redundant bit ~~corresponds to~~having a negated parity of the parity of the

seventh data bit, ~~of~~ the sixth data bit, ~~of~~ the fifth data bit, ~~of~~ the fourth data bit, ~~of~~ and the first data bit;

(f) a second redundant bit ~~corresponds to~~having negated parity of the parity of seventh data bit, ~~of~~ the sixth data bit, ~~of~~ the third data bit ~~of~~ the second data bit, ~~of~~and the zero data bit;

(g) a first redundant bit ~~corresponds to~~having a -negated parity of the seventh data bit, ~~of~~ the fifth data bit, ~~of~~ the fourth data bit, ~~of~~ the third data bit, ~~of~~and the zero data bit; and

(h) a zero redundant bit ~~corresponds to~~having a negated parity of the parity of the sixth data bit, ~~of~~ the fourth data bit, ~~of~~ the third data bit, ~~of~~ the second data bit, ~~of~~and the first data bit.

7. (Currently Amended)~~A~~ The memory component or memory module as claimed in claim 4, ~~characterized in that~~wherein the data bits and the redundant bits together correspond to the physical states.

8. (Currently Amended)~~A~~ The memory component or memory module as claimed in claim 1, ~~characterized in that~~wherein the memory cell matrix is assigned at least one source, at least one bit line, at least one word line and at least one control gate.

9. (Currently Amended)~~A~~ The memory component or memory module as claimed in claim 1, ~~characterized in that~~wherein the memory component or memory module is configured as an ~~E[rasable]P[rogrammable]R[ead]O[nly]M[emory]~~ Erasable

Programmable Read Only Memory (EPROM), as an ~~E[lectrically]E[rasable]P[rogrammable]R[ead]O[nly]M[emory]~~ Electrically Erasable Programmable Read Only Memory (EEPROM), as a Flash memory, as a ~~R[ead]O[nly]M[emory]~~ Read Only Memory (ROM)or as a ~~R[andom]A[ccess]M[emory]~~ Random Access Memory (RAM).

10. (Currently Amended) The use of at least one electronic memory component or memory module as claimed in claim 1 in order to detect and/or label invalid physical states or physical states that are special~~ in some other way~~.

11. (Currently Amended)A method of operating at least one electronic memory component or memory module~~, in particular as claimed in claim 1~~, comprising ~~in which~~mapping physical states representing regular data ~~are mapped~~ by ~~means of at least one~~a mapping function between physically implemented bits (P) and logically read bits (K) that describes at least one error correction code, and ~~for example at least one Hamming code, characterized in that~~identifying at least one ~~further~~additional physical state in the form of at least one exceptional or special state (S,L) of data other than regular data for distinguishing unwritten memory blocks from previously written memory blocks ~~in~~ by an associated~~ the~~ error correction code ~~can be detected, encoded and/or~~ indicated by ~~means of~~ the mapping function.

12. (Currently Amended) ~~A~~ The method as claimed in claim 11, ~~characterized in that~~wherein the ~~further~~additional physical state can be detected, encoded and/or indicated on the basis of its bit pattern~~, even in the case of~~ by an error detection and/or correction operation ~~which can be used only to a limited extent~~ for use with the regular data.

13. (Currently Amended)~~A~~ The method as claimed in claim 11, ~~characterized by~~ comprising at least one redundant data encoding operation.

14. (Currently Amended)~~A~~ The method as claimed in claim 11, ~~characterized in that~~wherein at least one Hamming code ~~intended~~ for correcting one-bit errors in the memory cell area and having a Hamming distance of 3 is selected as the error correction code, so that each valid ~~code word or data~~ word differs from any other ~~code word or data~~ word in at least three bits, and in that for each eight-bit ~~code word or data~~ word additionally at least four redundant bits are provided, so that twelve-bit ~~code words or data~~ words are formed.

15. (Currently Amended) ~~A~~ The method as claimed in claim 14, ~~characterized in that~~further comprising –operating the Hamming code ~~is selected~~ such that each valid twelve-bit ~~code word or data~~ word has at least two ~~set~~ bits that are set at a predetermined level and/or at least two ~~erased~~ bits that have been erased, so that each valid twelve-bit ~~code word or data~~ word has a minimum Hamming distance of 2 for special states in which all bits of a byte are set or in which all bits of a byte are erased.

16. (Currently Amended) ~~A~~ The method as claimed in claim 14, ~~characterized by at least~~ wherein the mapping one ~~twelve-fold~~ twelve input "and" operation to which the data bits and the redundant bits ~~can be~~ are applied, and/or by at least one ~~twelve-fold~~twelve input "nor" operation to which the data bits and the redundant bits ~~can be~~are applied for detecting the exceptional or special state in the error correction code.

17. (Currently Amended)~~A~~ The method as claimed in claim 14, ~~characterized in that~~wherein the four redundant bits in the test mode, which also comprises states in which all bits of a byte are set at a predetermined level or in which all bits of a byte are erased, are selected as follows:

~~third redundant bit corresponds to parity of the seventh data bit, of the sixth data bit of the fifth data bit of the fourth data bit of the first data bit second redundant bit corresponds to parity of the seventh data bit, of the sixth data bit of the third data bit of the second data bit, of the zero data bit first redundant bit corresponds to parity of the seventh data bit, of the fifth data bit of the fourth data bit of the third data bit of the zero data bit zero redundant bit corresponds to parity of the sixth data bit of the fourth data bit of the third data bit of the second data bit, of the first data bit; and/or in the normal mode are selected as follows: third redundant bit corresponds to negated parity of the seventh data bit, of the sixth data bit of the fifth data bit of the fourth data bit of the first data bit second redundant bit corresponds to negated parity of the seventh data bit, of the sixth data bit of the third data bit of the second data bit, of the zero data bit first redundant bit corresponds to negated parity of the seventh data bit, of the fifth data bit of the fourth data bit of the third data bit of the zero data bit zero redundant bit corresponds to negated~~

~~parity of the sixth data bit of the fourth data bit of the third data bit of the second data bit, of the first data bit~~

a) a third redundant bit R3 having a same parity as a seventh data bit, a sixth data bit, a fifth data bit, a fourth data bit and a first data bit;

(b) a second redundant bit R2 having a same having a same parity as the seventh data bit, the sixth data bit, a third data bit, a second data and a zero data bit;

(c) a first redundant bit R1 having a same parity as the seventh data, the fifth data bit, the fourth data bit, the third data bit, and the zero data bit;

(d) a zero redundant bit R0having a same parity as the sixth data bit, the fourth data bit, the third data bit, the second data bit and the first data bit; and/or

wherein in a normal mode are the twelve bit words are selected as follows:

(e) a third redundant bit having a negated parity of the parity of the seventh data bit, the sixth data bit, the fifth data bit, the fourth data bit, and the first data bit;

(f) a second redundant bit having negated parity of the parity of seventh data bit, the sixth data bit, the third data bit the second data bit, and the zero data bit;

(g) a first redundant bit having a negated parity of the seventh data bit, the fifth data bit, the fourth data bit, the third data bit, and the zero data bit; and

(h) a zero redundant bit having a negated parity of the parity of the sixth data bit, the fourth data bit, the third data bit, the second data bit, and the first data bit.

18. (Currently Amended) ~~A~~ The method as claimed in claim 14, ~~characterized in that~~wherein the data bits and the redundant bits together correspond to the physical states.

19. (Currently Amended) An error correction circuit, implemented or integrated in at least one electronic memory component or memory module as claimed in claim 1 ~~and/or operating in accordance with the method as claimed in claim 11~~.

20. (Currently Amended) ~~An~~ The error correction circuit as claimed in claim 19, characterized by at least one computation unit which is provided for computing or determining redundant bits, at least one multiplexing unit to which noninverted redundant bits ~~can be~~ are applied in the test mode and/or to which inverted redundant bits ~~can be~~are applied in the normal mode being connected downstream of said computation unit.

21. (Currently Amended) ~~An~~The error correction circuit as claimed in claim 19, ~~characterized by~~ further comprising at least one ~~twelve-fold~~twelve input "and" gate to which the data bits and the redundant bits ~~can be~~are applied, and/or ~~by~~ at least one ~~twelve-fold~~twelve input "nor" gate to which the data bits and the redundant bits ~~can be~~are applied for detecting the exceptional or special state in the error correction code.

22. (Currently Amended)~~An~~ The error correction circuit as claimed in claim 19, ~~characterized by~~ comprising at least one multiplexing unit to which the redundant bits ~~can be~~are applied, which multiplexing unit is provided for switching in the test mode, the nonnegated redundant bits and/or in the normal mode, the negated redundant bits through to at least one correction unit connected downstream of the multiplexing unit.

23. (Currently Amended)~~An~~ The error correction circuit as claimed in claim 20, ~~characterized by~~ comprising at least one inverter unit connected upstream of that input of the multiplexing unit ~~which is provided~~ for the normal mode.

24. (Currently Amended)~~An~~ The error correction circuit as claimed in claim 22, ~~characterized in that~~wherein the correction unit computes and/or determines the expected redundant bits from the data bits and compares these expected redundant bits with the redundant bits switched through by the multiplexing unity, said redundant bits being nonnegated in the test mode and negated in the normal mode.

25. (Currently Amended)A smart card ~~The use of the method as claimed in claim 11 in order to implement at least one additional safety feature in at least one smart card, in particular in at least one smart card controller unit~~ comprising a controller including a memory component or memory module as recited in claim 1.